REMARKS

This responds to the Office Action mailed on February 10, 2004.

Claims 1, 6, 13, and 18 are amended, claims 49-50 are canceled without prejudice or disclaimer, and no claims are added; as a result, claims 1-48 are now pending in this application.

§103 Rejection of the Claims

Claims 1-5 and 13-17 were rejected under 35 USC § 103(a) as being unpatentable over Rengarajan et al. (U.S. Patent No. 6,323,103) in view of Choi et al. (U.S. Patent No. 5,750,424) and Komori et al. (U.S. Patent No. 5,455,437). Claims 6-12 and 18-24 were rejected under 35 USC § 103(a) as being unpatentable over Rengarajan et al. in view of Komori et al.

The pending office action states that, "Rengarajan et al. teach forming an n-well 30 in a p-well 10 comprised of the wafer, which comprises another transistor 24A. Furthermore, Komori et al. teach forming wells of one conductivity within wells of other conductivities in order to isolate the devices." The rejection further asserts that the "Pch Tr" of Komori is taught to be outside the first conductivity well region 4. Applicant respectfully traverses the rejection for at least the following reasons.

As noted by the Examiner, Rengarajan appears to show a p-type substrate 10, not a p-well. Applicant respectfully submits that a well within a substrate is distinguishable from a substrate that is merely doped with one impurity or another. As noted by the Examiner, and Komori, one distinguishing feature of wells is that they are frequently used to isolate devices from the substrate. Applicant is therefore unable to equate a doped wafer with a well that is formed within a substrate. Rengarajan does not show forming a first conductivity type semiconductor well in the first conductivity type well region, the first conductivity well region being located over a portion of a single second conductivity type semiconductor well, wherein the second conductivity type semiconductor well is sized to accommodate at least one transistor outside the first conductivity well portion. Further, Rengarajan does not show forming a second conductivity type semiconductor well in a semiconductor substrate using a single mask.

Komori appears to show a p-well 4 in a first n-well 6. Komori further appears to show a second separate n-well 5 adjacent to the n-well 6. The n-well 5 is formed in a separate masking

step (Figure 7c) Komori appears to utilize a number of masking steps [Figures 7(a) - 7(d)] in the formation of the number of wells. Komori does not show forming a first conductivity type semiconductor well in the first conductivity type well region, the first conductivity well region being located over a portion of a single second conductivity type semiconductor well, wherein the second conductivity type semiconductor well is sized to accommodate at least one transistor outside the first conductivity well portion. Further, Komori does not show forming a second conductivity type semiconductor well in a semiconductor substrate using a single mask.

In contrast, claims 1 and 6, as amended, include forming a first conductivity type semiconductor well in the first conductivity type well region, the first conductivity well region being located over a portion of a single second conductivity type semiconductor well, wherein the second conductivity type semiconductor well is sized to accommodate at least one transistor outside the first conductivity well portion. Further in contrast, claims 13 and 18, as amended, include forming a second conductivity type semiconductor well in a semiconductor substrate using a single mask.

Applicant's specification discusses disadvantages of using a number of masks on page 2, lines 12-17. Applicant's specification further discusses advantages of claimed configurations such as a reduction in a number of masks on page 9, lines 21-30.

Applicant respectfully submits that the additional reference of Choi fails to cure the deficiencies of Rengarajan and Komori as outlined above.

Because the cited references, either alone or in combination, do not show every element of Applicant's independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection are respectfully requested with respect to Applicant's independent claims 1, 6, 13, and 18. Additionally, reconsideration and withdrawal of the rejection are respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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Date 4-12-04

By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 12 day of April, 2004.

Tina Kohut
Name

Signature